Amendments to the Claims:

The following listing of claims will replace all prior versions, and listings, of claims in the application:

1. (Original) A semiconductor integrated circuit comprising:

a semiconductor substrate with a device formation region on a surface thereof, the device formation region having a first conductivity-type;

an anti-fuse comprising:

a first isolation region including an insulating material layer buried in a surface of the device formation region;

diffusion regions formed on the surface of the device formation region at both sides of the first isolation region, the diffusion regions having a second conductivity-type different from the first conductivity-type; and

electrodes contacting the diffusion regions; and

a writing circuit formed on the surface of the semiconductor substrate, the writing circuit applying a writing voltage between the electrodes of the anti-fuse to change the anti-fuse from a non-conductive state to a permanently conductive state between the electrodes.

2. (Original) The semiconductor integrated circuit according to claim 1, wherein the first isolation region further includes a channel stop layer for preventing formation of an inversion layer in contact with a lower surface of the insulating material layer.

3. (Original) The semiconductor integrated circuit according to claim 1, further comprising a plurality of transistors and second isolation regions formed on the surface of the semiconductor substrate, the second isolation regions isolating the transistors from each other,

wherein the insulating material layer of the first isolation region is buried in the surface of the device formation region to a first depth, and each of the second isolation

regions includes a second insulating material layer buried in the surface of the semiconductor substrate to a depth substantially the same as the first depth.

4. (Original) The semiconductor integrated circuit according to claim 3, wherein the transistors include MOS transistors having source and drain diffusion regions of the second conductivity-type, a depth of the source and drain diffusion regions of the MOS transistors is substantially the same as that of the diffusion regions of the anti-fuse.

5. (Original) The semiconductor integrated circuit according to claim 1, wherein:

the anti-fuse further includes a low breakdown voltage region formed in an upper portion of the device formation region, the low breakdown voltage region contains dopant of the first conductivity-type with a concentration higher than that of a lower portion of the device formation region; and

the diffusion regions of the anti-fuse are formed in the low breakdown voltage region.

6. (Original) The semiconductor integrated circuit according to claim 1, wherein at least one of the electrodes is formed of aluminum or an aluminum alloy.

7. (Original) The semiconductor integrated circuit according to claim 1, wherein the device formation region is a well region formed in the surface of the semiconductor substrate.

8. (Original) A method for manufacturing a semiconductor integrated circuit on a surface of a semiconductor substrate, the method comprising:

forming an anti-fuse on the surface of the semiconductor substrate, the forming including:

forming a device formation region having a first conductivity-type on the surface of the semiconductor substrate, the device formation region having a first isolation region including an insulating material layer buried in a surface of the device formation region;

forming diffusion regions on the surface of the device formation region at both sides of the isolation region, the diffusion regions having a second conductivity-type different from the first conductivity-type, and

forming electrodes contacting the diffusion regions; and

forming a writing circuit on the surface of the semiconductor substrate, the writing circuit applying a writing voltage between the electrodes to change the anti-fuse from a non-conductive state to a permanently conductive state between the electrodes.

9. (Original) The method according to claim 8, wherein the first isolation region is formed by one of local oxidation of silicon (LOCOS) process and shallow trench isolation (STI) process.

10. (Original) The method according to claim 8, wherein the forming of the device formation region further includes adding at least one dopant of the first conductivity-type into the isolation region to form a channel stop region under the insulating material layer.

11. (Original) The method according to claim 8, further comprising forming a plurality of transistors and second isolation regions on the surface of the semiconductor substrate, the second isolation regions isolating the transistors from each other,

wherein the first isolation region of the anti-fuse is formed simultaneously with the second isolation regions.

12. (Original) The method according to claim 11, wherein the transistors include source and drain diffusion regions formed in the surface of the semiconductor substrate, and the source and drain diffusion regions of the transistors are formed simultaneously with the diffusion regions of the anti-fuse.

13. (Currently Amended) A semiconductor integrated circuit comprising:

a semiconductor substrate with a plurality of device formation regions on a surface thereof, the device formation regions having a first conductivity-type;

a plurality of anti-fuses formed in the respective device formation regions, each of the anti-fuses comprising a first isolation region including an insulating material layer buried in a surface of a corresponding one of the device formation regions, diffusion regions having a second conductivity type different from the first conductivity-type formed on the surface of the corresponding one of the device formation regions at both sides of the first isolation region, and electrodes contacting the diffusion regions, each of the anti-fuses being changeable from a non-conductive state to a permanently conductive state between the electrodes by applying a writing voltage between the electrodes; and

an internal circuit formed on the surface of the semiconductor substrate, the internal circuit being configured in a desired operational state by changing at least one of the anti-fuses to thea permanently conductive state.

14. (Original) The semiconductor integrated circuit according to claim 13, wherein each of the first isolation regions further includes a channel stop layer for preventing formation of an inversion layer in contact with a lower surface of the insulating material layer.

15. (Original) The semiconductor integrated circuit according to claim 13, wherein:

the internal circuit includes a plurality of transistors and a plurality of second isolation regions formed on the surface of the semiconductor substrate, the second isolation regions isolating the transistors from each other; and

the insulating material layer of each of the first isolation regions is buried in the surface of the corresponding one of the device formation regions to a first depth, and each of the second isolation regions includes a second insulating material layer buried in the surface of the semiconductor substrate to a depth substantially the same as the first depth.

16. (Original) The semiconductor integrated circuit according to claim 15, wherein the transistors include MOS transistors having source and drain diffusion regions of

the second conductivity-type, a depth of the source and drain diffusion regions of the MOS transistors is substantially the same as that of the diffusion regions of the anti-fuses.

17. (Original) The semiconductor integrated circuit according to claim 13, wherein:

each of the anti-fuses further includes a low breakdown voltage region formed in an upper portion of the corresponding one of the device formation regions, the low breakdown voltage region contains dopant of the first conductivity-type with a concentration higher than that of a lower portion of the corresponding one of the device formation regions; and

the diffusion regions of each of the anti-fuses are formed in the low breakdown voltage region of the corresponding one of the device formation regions.

18. (Original) The semiconductor integrated circuit according to claim 13, wherein the device formation regions are well regions formed in the surface of the semiconductor substrate.